Photocurrent Mapping of 3D CdSe/CdTe Windowless Solar Cells

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ABSTRACT: This paper details the use of scanning photocurrent microscopy to examine localized current collection efficiency of thin-film photovoltaic devices with in-plane patterning at a submicrometer length scale. The devices are based upon two interdigitated comb electrodes at the micrometer length scale prepatterned on a substrate, with CdSe electrodeposited on one electrode and CdTe deposited over the entire surface of the resulting structure by pulsed laser deposition. Photocurrent maps provide information on what limits the performance of the windowless CdSe/CdTe thin-film photovoltaic devices, revealing "dead zones" particularly above the electrodes contacting the CdTe which is interpreted as recombination over the back contact. Additionally, the impact of ammonium sulfide passivation is examined, which enables device efficiency to reach 4.3% under simulated air mass 1.5 illumination.

KEYWORDS: back contact, CdSe, CdTe, photovoltaic, 3D solar cells, SPCM
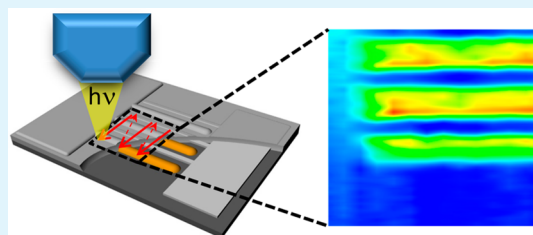
INTRODUCTION

Scanning photocurrent microscopy (SPCM) has been used to evaluate the local performance of solar cells by scanning a finely focused optical beam across the surface while monitoring device response. In contrast to electron beam induced current mapping techniques, SPCM compromises resolution; however, it provides direct translation to operating conditions in which both minority and majority carriers are generated.[1,2] With length scales defined by the light source and optics, SPCM can be used to study transport behavior in thin-film materials exhibiting micrometer-scale diffusion lengths and designs incorporating similar feature size. As such, SPCM has been used in studies exploring the impact of processing conditions, window layer thickness, accelerated aging and back contact treatments, performance and structural inhomogeneities, series resistance, grain boundaries, and pinholes for a mechanistic understanding and process optimization.[3] Recently, it has been used to evaluate photovoltaic performance of thin-film and nanowire-based devices with submicrometer resolution.[4,5]

This capability is relevant to efforts aimed at improved efficiency or utilization of more abundant, but typically lower quality, materials with light management strategies and advanced architectures that often include intricate nanoscale concepts. These approaches include plasmonic, quantum dot and nanowire-based devices that, while promising, are empirically challenging for a variety of reasons.[5−9] Contact and heterojunction structures that depart from conventional planar designs to yield improved performance are particularly appealing.[10] Critical to achieving better performance of all these platforms is an improved understanding of electron−hole pair generation in three-dimensional (3D) absorber materials and concomitant charge carrier transport.

This work explores a dual back contact geometry that imparts three dimensionality to thin-film CdTe photovoltaic devices. By relocating the front contact to the rear of the device, adjacent to the other contact in an interdigitated fashion, the associated window layer and its absorptive losses are eliminated. While a number of back contact geometry devices have been detailed in the literature for crystalline Si,[11−13] finer pitch electrodes consistent with the shorter carrier recombination lengths of thin-film materials impose a significant departure in terms of design and processing.[14−16] For thin-film devices in particular, the back contact geometry removes the requirement for a transparent conducting oxide contact and the need for a wide band gap n-type junction layer transparent to the illuminating light. The opportunity provided by the latter change is exemplified by the use of CdSe (band gap ≈ 1.75 eV) here and in a previous study of analogous CdTe/CdSe devices.[17] In this study, prepatterned substrates were utilized with site-selective electrodeposition to coat one electrode with CdSe and subsequent blanket deposition of CdTe via pulse laser deposition (PLD) completing the device; in the previous

study both CdSe and CdTe were electrodeposited. To probe 3D behavior and uniformity of quantum efficiency, these back contacted CdSe/CdTe devices were examined by SPCM, divulging a response with periodicity linked to that of the underlying wire contacts. The significance of recombination was also explored, with passivated devices exhibiting more evenly distributed collection in current maps and an approximately 150 mV increase of open-circuit voltage over that of unpassivated devices. Taken together, these findings suggest considerable promise for back contact geometries through electrode engineering and surface chemistry.

EXPERIMENTAL SECTION

Device Fabrication. Device fabrication started with the simultaneous patterning of the two interdigitated comb electrodes on oxidized silicon wafer substrates. The distance between the midlines of the adjacent wires of the two electrodes (pitch) is fixed at a value between 2 and 3 μm, while the wire width is fixed at a value between 1 and 2 μm. Electrode types are indicated as appropriate, the variants labeled using the designations found in Table 1 of ref 17. Two contact pads permit electrical access to all the wires. The wires are 4 mm long and the active area of each device a square, four millimeters on a side, giving 0.16 cm^2 of active area. In this study the electrodes were fabricated by a lithographic lift-off process from 50 to 100 nm thick iridium deposited by electron beam evaporation. Electrical measurements indicate the electrical resistance associated with conduction through all of the interdigitated wires in parallel is 10–20 Ω; the shunt resistance between the two interdigitated electrodes is initially greater than 10 MΩ prior to semiconductor deposition.

CdSe was electrodeposited on each device using an underpotential codeposition process[18,19] as detailed previously for CdS/CdTe[14] and CdSe/CdTe[17] back contact devices. Following the electrodeposition of CdSe the devices were rinsed in 18 MΩ·cm water, dried, and then annealed in a tube furnace at 500 °C for 5 min under a N$_2$ atmosphere.

CdTe was subsequently deposited by pulsed laser deposition using a KrF excimer laser with a wavelength of 248 nm. The laser pulse energy was set to 120 mJ, and the laser pulse frequency was held at 12 Hz. A Kurt J. Lesker CdTe target of 99.999% purity was used. (Certain commercial equipment, instruments, or materials are identified in this paper to specify the experimental procedure adequately. Such identification is not intended to imply recommendation or endorsement by the National Institute of Standards and Technology, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.) The substrate to target distance was set to 6 cm. The base pressure of the deposition system was 6.7 × 10^{-4} Pa (5 × 10^{-6} Torr). The substrate temperature was held at 200 °C during deposition; a rotating stage was used to improve uniformity.

After the CdTe deposition, methanol saturated with cadmium chloride (CdCl$_2$) was evaporated on the completed devices using a hot plate. Following a 10 min translation into the furnace, the coated devices were annealed at 400 °C for 10 min in a nitrogen plus oxygen environment to recrystallize the CdTe deposits and improve device performance. This annealing procedure is identical to that used for the CdSe/CdTe devices with electrodeposited CdTe and CdSe. Final processing involved immersion in 40 mass % (aq) ammonium sulfide ((NH$_4$)$_2$S) at room temperature for the indicated times.

Characterization Methods. The microstructure and composition of the materials in the devices were examined using a scanning electron microscope (SEM) equipped with an X-ray energy-dispersive spectroscopy (XEDS) analysis system. Planview images were taken without sample preparation, and cross sections were imaged from freshly cleaved samples.

The local external quantum efficiency (EQE) and photoluminescence (PL) measurements were collected with a Raman microscope system equipped with a 532 nm laser; the beam was turned on a minimum of 15 min prior to device measurements to ensure stability

during the measurements. The short-circuit current (I_{sc}) was monitored chronopotentiometrically with a CH Instruments potentiostat connected to the device by micromanipulator probes. The laser beam passed through a neutral density filter and 100× objective for focusing, and the light intensity at the device was measured with a Thor Laboratories PM100D laser power meter immediately after device measurements. Laser system power was maintained at 100% for high intensity measurements and at 50% for low intensity measurements. Measured laser output power at the sample for these conditions was on the order of 1 nW and 1 μW. On the basis of an approximate beam diameter of 1.5 μm, incident power densities are several times larger than, but of the order of, 0.1 and 100 W/cm^2, respectively. The lower intensity beam thus has a power density similar to the 0.1 W/cm^2 power density of spectrally integrated air mass 1.5 solar insolation (AM1.5).

The piezoelectric stage was manually manipulated for local current−voltage (I−V) measurements. For mapping, it was scanned using a 0.2 μm resolution that limited drift and 1−2 μm offsets of successive scans for area measurements. Edge diffusion effects are likely significant because the illumination spot is similar in size to relevant features and characteristic transport lengths. For this reason, the absolute values in the EQE maps reported here should not be considered directly comparable to standard external quantum efficiency measurements.

RESULTS AND DISCUSSION

Device Structure. The design and fabrication of these dual back contacted devices depart significantly from planar devices in that it starts with prefabricated wire contacts upon which the semiconducting materials are subsequently deposited. This results in a fully exposed absorber surface (Figure 1a) that lifts window layer absorption restrictions. However, constraints are imposed on the electrode material, which must survive the thermal processing required to fabricate high-quality absorbers including CdTe. A number of solid materials or coated structures can be envisioned with such requirements in mind.
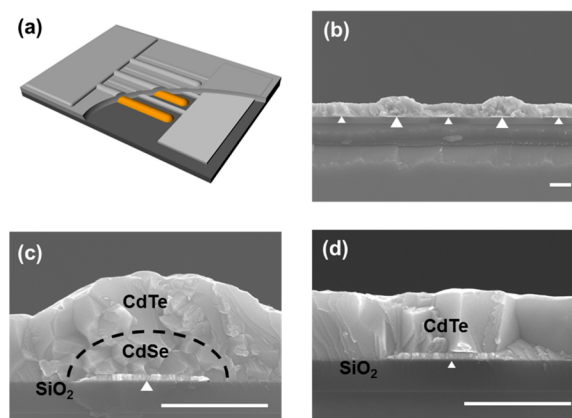

Figure 1. (a) Schematic of the interdigitated back contact CdSe/CdTe device on an insulating substrate (dark gray). The two interdigitated electrodes are pictured with: the overlying CdTe (medium gray) removed from a portion of the device, the CdSe on one electrode (gold), and the underlying Ir wires of the other electrode with the contact pad connecting them (light gray). (b) Cross-section SEM image of a CdSe/CdTe device with 2.5 μm pitch and 1 μm wide (type II−I) by 0.05 μm tall wire contacts, exhibiting periodicity twice the electrode pitch that results from the CdSe deposit on every other wire (i.e., on one of the two interdigitated electrodes). Arrows mark the locations of the wire contacts. (c) Higher magnification images of a CdSe-coated wire contact with overlying CdTe and the heterojunction delineated, and (d) the CdTe wire contact. Scale bars are 1 μm.

Iridium electrodes were used here for facile processing, the large work function (approximately 5.5 eV[20]) that should be reasonably well suited for the CdTe contact, and stability of the metal−semiconductor interfaces (CdTe/Ir and CdSe/Ir).[17] A Schottky junction at the n-CdSe/Ir interface is likely detrimental to device performance, and it is anticipated that a shallower work function material or band alignment optimization will improve performance. Figure 1 shows SEM images of portions of a cross-sectioned CdSe/CdTe device after full thermal processing. The CdSe electrodeposited on every other wire contact (i.e., one of the two interdigitated electrodes) manifests as a thicker device over alternating wire contacts. Finer CdTe grains are obtained on top of the CdSe, whose presence has been previously confirmed by XEDS.[17] The reason for the finer CdTe grain size is not known; however, possible reasons include lattice matching to the CdSe during the deposition or interdiffusion during the anneal.

In planar CdS/CdTe solar cells, annealing with CdCl$_2$ can increase grain size, relax stresses, induce interdiffusion between the CdS and CdTe, and facilitate impurity gettering to grain boundaries, thereby improving electrical properties and spectral response in the UV range.[21] With the back contact CdSe/CdTe devices, annealing with CdCl$_2$ also induces significant CdTe recrystallization and grain growth as well as improved crystalline quality of the two semiconductors. The recrystallized microstructure has been previously detailed[17] and is associated with improved solar cell behavior.

Device Performance. Devices were characterized using simulated AM1.5 illumination to obtain current density versus voltage (J−V) behavior and using a spectrally filtered light source to obtain EQE. Both measurement systems were calibrated using a NIST-calibrated silicon photodiode. Performance of representative CdSe/CdTe devices is summarized in Table 1, with superior J−V and EQE data shown in Figures 2 a

Table 1. Performance Parameters for Three Interdigitated Back Contact CdSe/CdTe Solar Cells Exhibiting a Range of Efficiencies As Annealed[a]

electrode pitch/width/height (μm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF	η (%)	R_{Shunt} (Ω)	R_{Series} (Ω)
2.5/1.5/0.07	488	13.8	44	2.96	2851	113
2.5/1.5/0.05	442	14.5	38.6	2.47	1549	113
2.5/1.5/0.05	456	14.0	36	2.27	1025	168

[a]All devices were fabricated with 0.6 μm of PLD CdTe and a CdSe thickness of ≈0.3 μm based on 20 min electrodeposition time. The indicated electrode pitch and width are for type II−II devices. Performance variation between nominally identical devices likely arises from differences between the lithographically defined electrodes or the electrochemically deposited CdSe.

and b, respectively. The back contact devices studied differ in the pitch of adjacent electrode wires, the width of the wires, and/or the gap between the wires. The CdSe is ≈0.3 μm thick on every other wire contact with an ≈0.6 μm thick overlayer of CdTe completing the electrode/CdSe/CdTe/electrode structure of the devices. Series resistance during operation was extracted from dV/dI evaluated at the open-circuit voltage (V_{oc}) under AM1.5 illumination, while shunt resistance was extracted from dV/dI evaluated near zero voltage. On the basis of the measured series resistances of the best devices, the resistance of the underlying wire contacts likely impairs their performance only modestly.

From Table 1, as-annealed PLD CdTe devices exhibit open-circuit voltages similar to those of devices with electrodeposited (ECD) CdTe. On the other hand, they exhibit short circuit current densities (J_{sc}) values approaching and exceeding 14 mA/cm^2, substantially higher than the 8 mA/cm^2 of similar devices fabricated with ECD CdTe.[17] The PLD CdTe also reduces the previously noted variation of J_{sc} with both the width of the wire contacts and the gap between them. These results suggest carrier lifetimes are significantly longer in the PLD CdTe than in the ECD CdTe. The EQE of these devices, reaching 39% (Figure 2b), also substantially exceeds the 29% value achieved with devices fabricated with ECD CdTe.[17] The back contact geometry yields relatively constant EQE response at all energies above the CdTe bandgap; in contrast to the EQE dropoff observed above the CdS bandgap in planar devices with CdS window layers, in these devices there is no similar drop-off above the CdSe bandgap (709 nm). The modest decline of EQE in the ultraviolet range (beyond that underlying the overall sub-40% EQE response across the spectrum) also suggests improved quality CdTe; because this light is absorbed farther from the space-charge region located at the buried n/p junction in this geometry, EQE will be especially sensitive to bulk as well as surface recombination. In this regard, the shape of the EQE profile, with a peak near 650 nm, also suggests absorption losses at longer wavelengths. A similar decrease of EQE at longer wavelengths is also observed with planar "ultrathin film" devices having similar (0.68 μm) CdTe thickness.[22]

Scanning Photocurrent Microscopy. In an effort to understand the charge transport and improved current density, these devices were also characterized using the focused 532 nm laser beam. The I−V response was evaluated for illumination over a CdSe wire contact, over a CdTe wire contact, and over the gap midway between them. The data curves are shown along with the dark current in Figure 3a. The locations are shown schematically in Figure 3b and as a composite of images of the actual illuminated surface in Figure 3c. For a laser power of 3.5 μW, I_{sc} with the beam placed between the contacts corresponds to a quantum efficiency of ≈23%.

Spatial variation of the device response is explored further by mapping I_{sc} with the piezoelectric stage under 4.4 μW of laser power. The scan sequence is depicted schematically in Figure 4 a. Peak response in the resulting EQE map (Figure 4b i) extends from the edges of the wire contacts into the gaps between them. There is minimal response over the contact wires, consistent with the I_{sc} values in Figure 3. A single line profile, Figure 4 c, reveals current collection is associated with illumination between the wire contacts with minimal collection occurring when illumination is above them. The EQE valleys are asymmetric, with somewhat more efficient current collection for illumination over the CdSe coated wire. Significantly, scanning at 10 nW of laser power, corresponding to 440-fold lower light intensity similar to that of spectrally integrated AM1.5 solar insolation, generates a much different area (Figure 4b ii) and line (Figure 4d) response. The shaded regions in Figures 4c and d cover the periodicity of the device (i.e., twice the 3 μm pitch of the wire contacts); integrated efficiency over these regions is ≈60% higher with the lower light intensity due to substantially improved current collection for illumination over the CdSe contact. This behavior is expected to be more representative of device operation and suggests that, under these conditions, current collection is predominantly limited by proximity to the n\p junction.
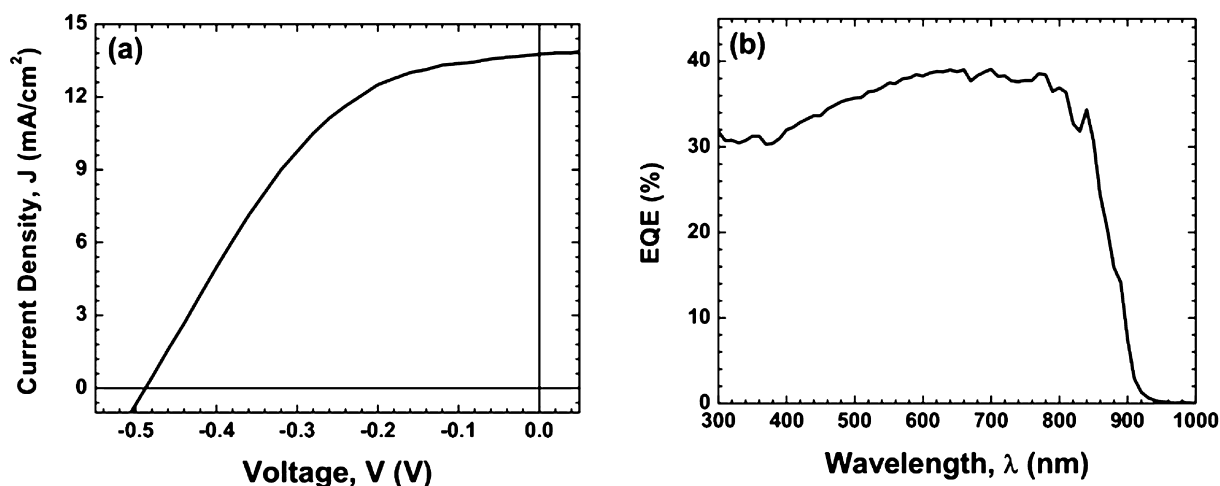
Figure 2. (a) Current density versus voltage ($J-V$) response under A.M. 1.5 illumination and (b) external quantum efficiency (EQE) versus wavelength of the illuminating light for interdigitated back contact CdSe/CdTe solar cells after annealing. The data come from the first two devices in Table 1, respectively.
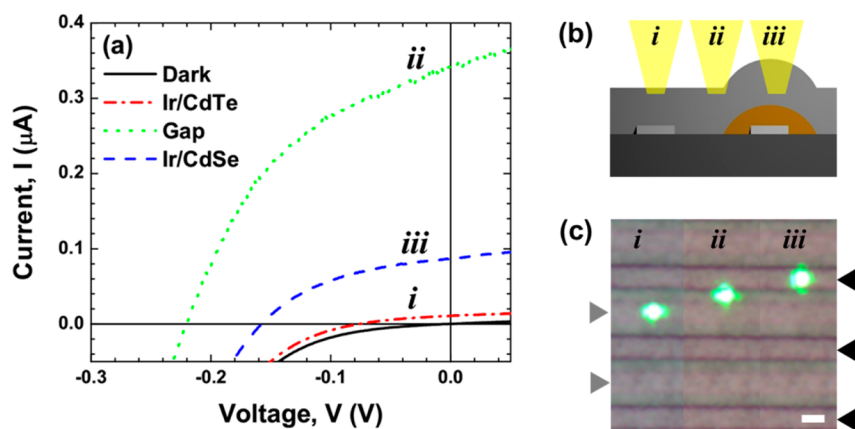

Figure 3. (a) Current versus voltage ($I-V$) response for a device with 3 μm pitch and 2 μm wide (type III–II) by 0.1 μm tall wire contacts under 3.5 μW laser power at 532 nm localized over the CdSe (*i*) and CdTe (*ii*) wire contacts and between them (*iii*). (b) Schematic cross-section showing the locations of the three measurements on the back contacted CdSe/CdTe solar cell. (c) Superimposed optical images showing actual illumination spots for the measurements. Arrows indicate the locations of both the CdSe (larger black arrows) and CdTe (smaller gray arrows) wire contacts; the locations of the wires contacting the CdSe are easily distinguished by the added height of the CdSe. The wires contacting the CdTe are faintly visible midway between them. Scale bar is 1 μm.

Front surface recombination likely aggravates losses in this geometry in particular for two reasons: (1) exposed surface area is larger than junction and electrode contact area combined, and (2) a significant volume of CdTe over the CdTe/Ir wire contact and in the gap between wire contacts is in closer proximity to the surface than to the junction or contact. For these reasons, the impact of surface recombination on device performance was examined using ammonium sulfide treatments that have been previously shown to passivate CdTe and GaSb surfaces thereby extending minority carrier lifetimes.[23,24] Figure 5 presents $J-V$ curves under uniform AM1.5 illumination and SPCM maps of local EQE for a device before (*i*) and after (*ii*) passivation. The two $J-V$ curves in Figure 5a are very similar in shape, with corresponding fill factors of 39.4% (*i*) and 41.6% (*ii*) but exhibit ≈35% increase of both J_{sc} and V_{oc} after passivation. The increase in J_{sc} in particular is reflected in the SPCM maps by increased EQE response. The effective diffusion lengths taken from semilog plots of the photocurrent versus the distance from the CdSe junction[25] increase by more than 20% albeit with unquantified uncertainties arising from

variations in the grain boundaries, beam spot size, as well as drift during the line scans.

While passivation increased the V_{oc} and efficiency of all devices, J_{sc} enhancement appeared to reach an upper limit near 15 mA/cm². This is illustrated by the data in Figure 6a, where the optimally passivated J_{sc} values exhibit less scatter than those of the original unpassivated devices. When the passivation process is performed in 15 s increments (Figure 6b), J_{sc} declines modestly or is stable for devices with higher initial values, while devices with lower initial values exhibit a continuous increase of J_{sc}. At 45 s the J_{sc} values have converged at a common, maximum value. This optimum passivation time varied over approximately a 30 s range for different devices; however, a decrease of J_{sc} was increasingly severe for more extended passivation times. Conversely, V_{oc} (Figure 6c) generally increased with passivation time, even for extended durations (120 s). With some variation between devices, an increase of V_{oc} during passivation was generally similar to the ≈150 mV increase exhibited by these devices (Figure 6c). The fill factors for the devices (Figure 6d) follow a similar trend as
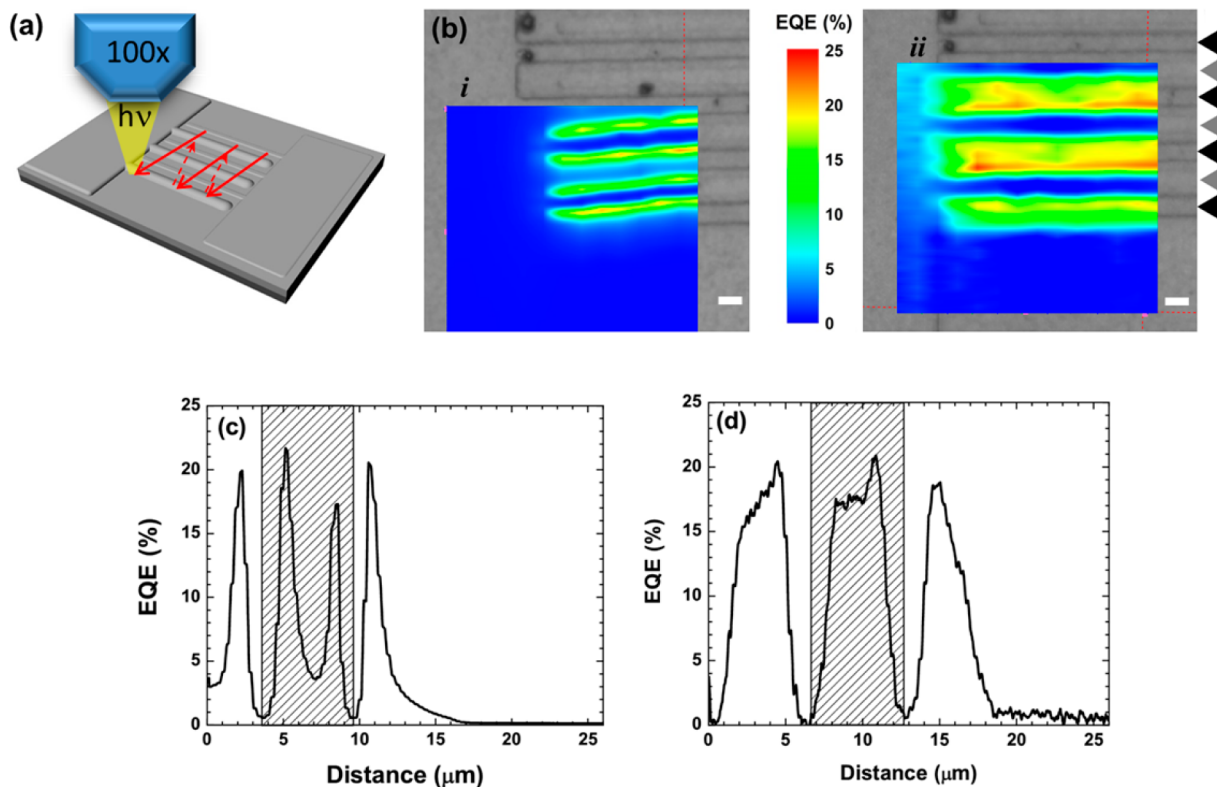
Figure 4. (a) Schematic of scanning photocurrent microscopy using a focused 532 nm laser. (b) Photocurrent maps under short-circuit conditions of the same device (type III−II) and location (note features at top) for localized illumination with (*i*) 4.4 μW laser power and (*ii*) 10 nW laser power. Representative line scans from each map are shown in (c) and (d), respectively. Arrows mark the locations of the wire contacts. Scale bars are 1 μm.
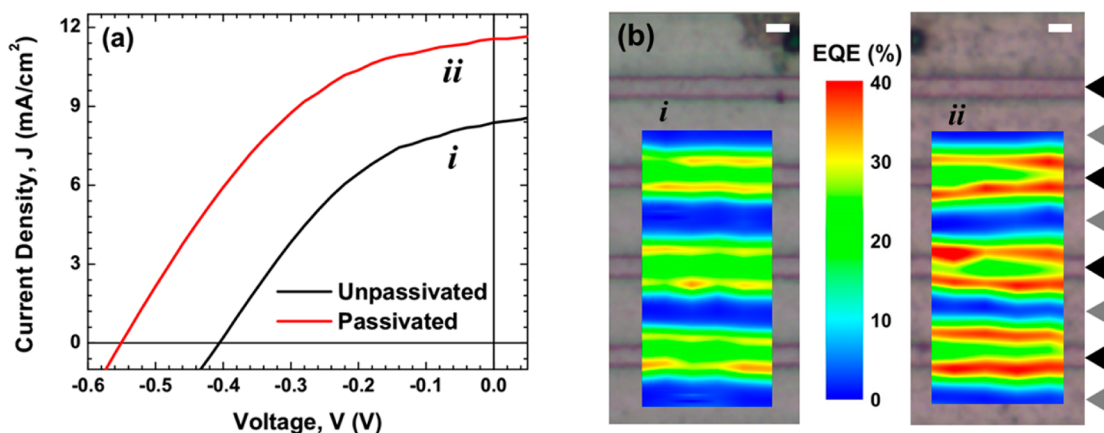

Figure 5. (a) Current density versus voltage response under A.M. 1.5 illumination of back contacted CdSe/CdTe device with 3 μm pitch and 1 μm wide (type III−I) by 0.05 μm tall wire contacts before and after passivation in 40% $(NH_4)_2S$ for 45 s. (b) EQE maps obtained by scanning photocurrent microscopy of a region of the same specimen under short-circuit conditions (*i*) before and (*ii*) after passivation treatment using a focused 532 nm laser with 2.3 nW power. Locations of wire contacts are indicated. Scale bars are 1 μm.

V_{oc} but with more modest increase. The cumulative impact of these changes is a 60 to 80% increase in power conversion efficiency, the highest efficiency device fabricated (type II−II) reaching a maximum efficiency of 4.3% after 45 s of passivation.

The improved performance, as well as its time-dependent variation, can be linked to chemical and physical changes occurring to the absorber during the passivation process. In particular, previous studies by X-ray photoelectron spectroscopy of ammonium sulfide treated CdTe surfaces have shown the process removes residual TeO_3 and neutralizes dangling bonds with the formation of surface CdS.[23] Photoluminescence was used here to look for changes in recombination associated with

the passivation process. Figure 7a shows the room-temperature photoluminescence spectra from a CdTe absorber pre- and post-passivation. The $CdCl_2$ annealed CdTe surface (unpassivated) displays a low and broad photoluminescence signal centered at 823 nm (1.51 eV) that is associated with the CdTe bandgap. The signal from the bandgap is nearly matched in intensity by luminescence from a defect band at longer wavelength. The passivation process nearly eliminates luminescence from the defects, and the response from the bandgap increases substantially. It also becomes narrower, indicating increased lifetime, with a full width half-maximum of 33 nm. These values, very close to the 824 and 30 nm values obtained
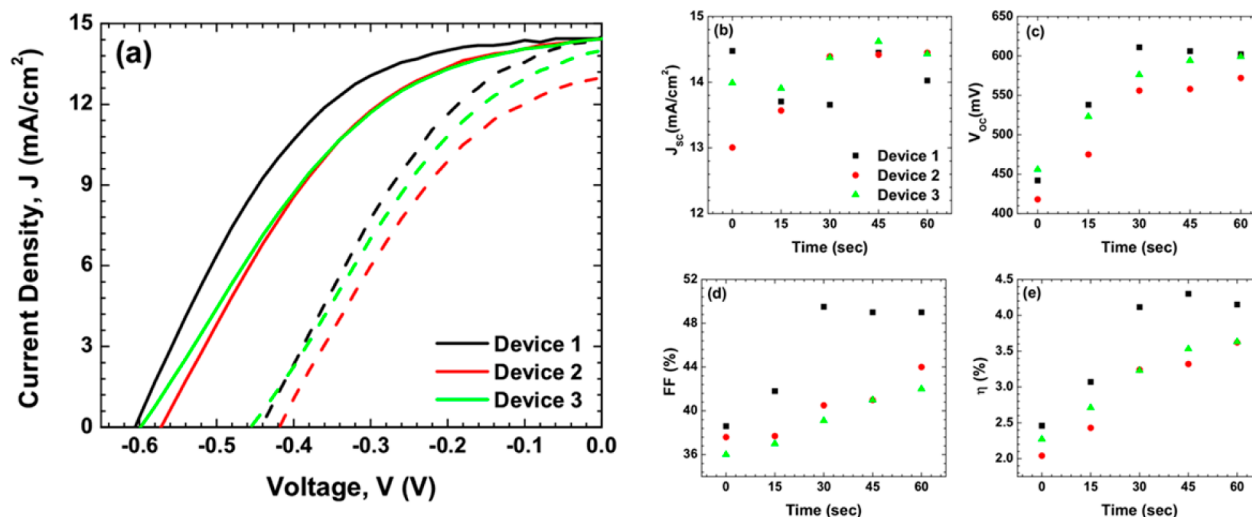
Figure 6. (a) Effect of passivation on J–V response under A.M. 1.5 illumination is shown for three devices after passivation for 45, 60, and 60 s, in order of device number. Devices 1 and 3 are type II–II, and device 2 is type I (2 μm pitch and 1 μm contact wire width); all devices have 0.05 μm tall contact wires. The impact of cumulative passivation time on (b) J_{sc}, (c) V_{oc}, (d) fill factor, and (e) power conversion efficiency is shown for the same devices. All three exhibit maximum J_{sc} after 45 s, with maximum efficiencies (for the examined passivation times) at 45 or 60 s.
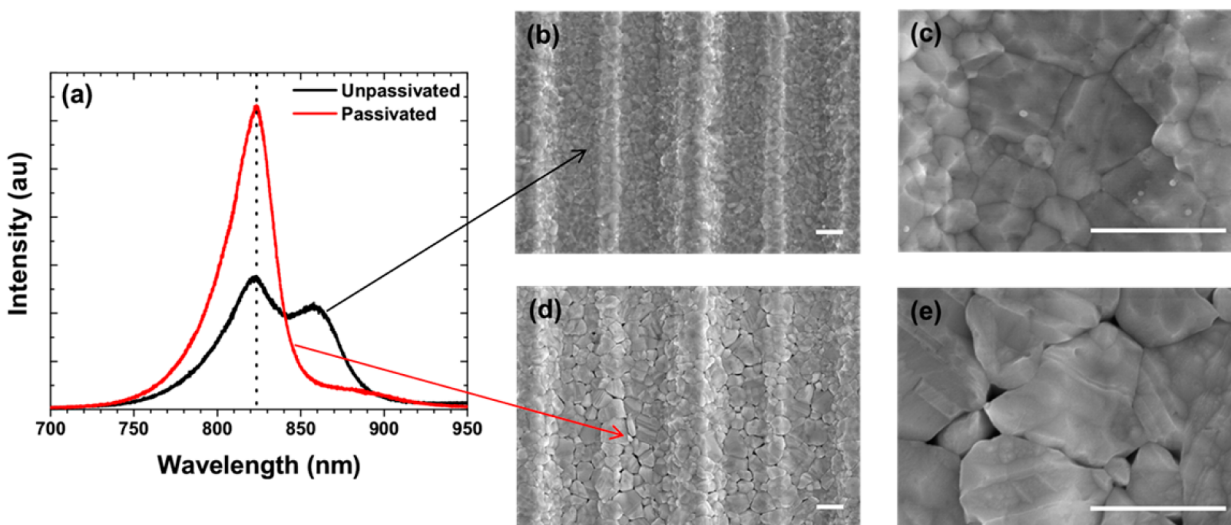

Figure 7. (a) PL spectra of a device (type III–II) before and after passivation in $(NH_4)_2S$ for 45 s. Planview SEM images of another back contact device (type III–I) with taller (ruthenium) contact wires both before (b, c) and after (d, e) passivation. The locations of the underlying electrode wires are evident, the associated topography especially pronounced over the CdSe-coated wire. Scale bars are 1 μm.

from annealed CdTe films grown by molecular beam epitaxy on sapphire,[26] are indicative of high quality material.

Structural changes arising from the passivation are well illustrated by the planview images in Figure 7b–e comparing the device surface before and after the 45 s passivation treatment. The surface of the device after the $CdCl_2$ anneal but prior to passivation is shown at lower magnification in Figure 7b; the fine-grained CdTe surface exhibits undulations marking the underlying wire contacts with CdSe on every other one. Higher magnification images confirm the presence of numerous small grains on the unpassivated surface (Figure 7c). The passivation process makes the grain boundaries more distinct, suggesting increased grain size at low magnification (Figure 7d). Larger grains on the passivated surface, delineated by dissolution of CdTe from the grain boundaries along with the smaller surface grains, are evident at higher magnification (Figure 7e). Images of cross-sectioned devices reveal the grain

boundary etching can penetrate more than 100 nm into the CdTe absorber (not shown).

Discussion. Quantitative understanding requires modeling such as has been previously undertaken for this geometry[14,17] and other 3D patterned photovoltaic geometries such as nanopillars.[6,8,27] Nonetheless, the data support several tentative conclusions.

As per Figure 4b ii, under low laser power that yields AM1.5-like illumination, locally defined EQE is largely dictated by the intrinsic diffusion length in the absorber; thus collection decreases as the distance from the junction increases. In contrast, a 440-fold increase in laser power results in substantial accumulation of holes over the CdSe/CdTe interface as electrons are pulled across the depletion layer to the Ir wire contact; collection of holes from the CdTe over the Ir contact leaves behind an analogous layer of rejected electrons over that contact. In both locations, because recombination scales with

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the product of holes and electrons, local carrier lifetimes drop and EQE decreases. Under uniform illumination the same shielding occurs, but with a distribution of rejected carriers associated with their diffusion across the surface of the electrode toward the gap and the appropriate contact. Illumination between wire contacts generally results in efficient lateral separation of holes and electrons by the laterally oriented depletion field originating from the vertically oriented CdSe/CdTe interface at the end of the coated contact.

The data in Figures 6 and 7 concerning the passivation process suggest both positive and negative changes emerge as a function of passivation time. Among the beneficial effects are the etching of TeO_3 and smaller surface grains as well as the passivation of dangling bonds by sulfidization.[23,28] Both J_{sc} and V_{oc} increase as the passivation process eliminates recombination centers. It is also possible that the passivation process impacts grain boundaries within the CdTe as they relate to inversion conduction pathways used to describe the superior behavior of polycrystalline thin-film CdTe devices over their single-crystalline counterparts.[29,30] Countering this improvement, grain boundary etching reduces current collection by impeding carrier transport. While fine scale grooves have a negligible, if not advantageous, impact on the performance of planar devices, in these devices they result in longer diffusion paths for charge carriers, particularly those generated near the surface and thus most relevant for UV response. Taken together, the saturating benefits of recombination center passivation and/or modification of grain boundary properties with passivation time and the steady increase of grain boundary etching underlie the observed trends of J_{sc} and V_{oc} in Figure 6.

The experimentally observed upper limit on J_{sc} is strongly influenced by the dead zone above the CdTe wire contact, which constitutes up to one-third of the effective device area depending upon the electrode geometry. Excluding these dead zones, the J_{sc} would be close to values for ultrathin film devices, which are presently ≈50% higher.[31] The reduced junction and contact areas of these devices, being approximately 37−55% and 17−33%, respectively, of those in planar devices of equivalent planar area, might also impact performance. The device J_{sc} of 14 mA/cm^2 corresponds to a current density of approximately 25 mA/cm^2 at the junctions; the current densities exceed 50 mA/cm^2 at the contact interfaces. Low acceptor concentrations in the intrinsic CdTe are almost certainly impacting junction performance at these high local current densities.

The results suggest a number of possible changes for improved efficiency. Devices with higher aspect ratio and taller and narrower electrodes wires would reduce the amount of CdTe absorber over the CdTe wire contact, placing more in between the wire contacts where collection is more efficient. Such design would also increase the junction area. An asymmetric design where the wire contacts for the CdSe are wider than those for the CdTe might also be considered based on the asymmetry of the local EQE response in Figure 4b ii. Finer pitch wire contacts would reduce distances for carrier transport in general and reduce the buildup of rejected carriers over the wires themselves. Finally, a back contact field over the CdTe wire contact would improve collection and reduce recombination in this region.

CONCLUSIONS

This work demonstrates CdTe photovoltaic devices that use a back contact geometry and n-type CdSe. Device performance was improved over previously detailed devices by replacing electrodeposited CdTe with material deposited by pulsed laser deposition. The use of iridium as the electrode material permitted high-temperature annealing for improved semiconductor microstructure and n/p junction. Further improvement was obtained by passivating the CdTe. As a result, the back contact devices studied here exhibit efficiencies under AM1.5 illumination reaching 4.3%. The best devices exhibit short-circuit current under AM1.5 illumination exceeding 14 mA/cm^2, open-circuit voltage exceeding 600 mV, and/or fill factor of nearly 50%. External quantum efficiencies approach 40%, with only modest reduction at the largest and shortest wavelengths. Local measurement of EQE with submicrometer resolution yielded information on factors limiting device performance, providing guidance on changes that might improve performance.

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Notes
The authors declare no competing financial interest.

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